

5       **METHODS FOR MAKING SEMICONDUCTOR STRUCTURES HAVING HIGH-  
SPEED AREAS AND HIGH-DENSITY AREAS**

TECHNICAL FIELD

10       This invention relates generally to semiconductor structures. More particularly, it  
pertains to making semiconductor devices so these devices operate at high speed while having  
high density.

BACKGROUND OF THE INVENTION

15       In the making of certain semiconductor devices, modern semiconductor processes  
may require a p-type semiconductor material to be adjoined to an n-type semiconductor material,  
but not for the purpose of forming a diode. However, a diode is naturally formed when a p-type  
semiconductor material is adjoined to an n-type semiconductor material. This situation allows  
current to undesirably flow if the diode is activated by accident in certain areas of a  
semiconductor structure. This current may render a semiconductor device defective. One  
20       solution to this problem is to place a conductive material on top of the n-type semiconductor  
material and the p-type semiconductor material as illustrated in Figures 1A and 1B.

25       Figure 1A is a cross-sectional view taken from the front of a conventional  
semiconductor structure 10 and Figure 1B is a cross-sectional plan view of the conventional  
semiconductor structure 10. The semiconductor structure 10 includes a gate oxide layer 8 that  
overlies an n-channel active area 2, a field region 18, and a p-channel active area 20. The n-  
channel active area 2 includes a p-type well 22 containing highly doped n-type areas 4, as shown  
in Figure 1B. These highly doped areas 4 form a drain region and a source region of an n-  
channel transistor. The highly doped n-type areas 4 are doped with donor impurities. The p-  
channel active area 20 includes an n-type well 24 containing highly doped p-type areas 4, as  
30       shown in Figure 1B. The highly doped p-type areas 4 are doped with acceptor impurities, and  
these highly doped p-type areas 4 form a drain region and a source region of a p-channel  
transistor.

5           The n-channel active area 2 also includes an n-type polycrystalline silicon strip 10A forming a transistor gate for the n-channel transistor, and the p-channel active area 20 includes a p-type polycrystalline silicon strip 10B forming a transistor gate for the p-channel transistor. A gate cap 12, which is formed from a nonconductive material, overlies both the n-type polycrystalline silicon strip 10A and the p-type polycrystalline silicon strip 10A. A spacer 10 14 surrounds a portion of the semiconductor structure 10 as shown in Figure 1B. Both the spacer 14 and the gate cap 12 electrically isolate and structurally support the transistor gates from other conductive layers (not shown) in the semiconductor structure 10.

          In complementary semiconductor structures, such as CMOS, dual-doped polycrystalline silicon is used to simultaneously form p-channel and n-channel devices. 15 Particularly, an SRAM cell uses a single polycrystalline line to form a gate electrode for both the pull-up device and the pull-down device. This single polycrystalline line is dual-doped with both acceptor impurities and donor impurities shown as portions 10A, B in Figure 1A.

          The n-type polycrystalline silicon strip 10A abuts against the p-type polycrystalline silicon strip 10B. As explained hereinbefore, a diode may undesirably form from 20 the semiconductor/semiconductor contact of the n-type polycrystalline silicon strip 10A and the p-type polycrystalline silicon strip 10B. However, for CMOS SRAM cells ohmic contact (i.e., semiconductor/metal contact) is desired. Should a voltage of an appropriate magnitude and polarity be accidentally placed between the n-type polycrystalline silicon strip 10A and the p-type polycrystalline silicon strip 10B, current may undesirably flow.

25           One solution is to use a salicide process to strap a conductive stack 13 on top of the n-type polycrystalline silicon strip 10A and the p-type polycrystalline silicon strip 10B. This conductive stack 13 shorts the two types of polycrystalline silicon strips 10A, B so they are at the same potential. Therefore, undesirable current cannot flow, so the net current between the two types of polycrystalline silicon strips 10A, B is zero. The conductive stack 13 comprises a 30 tungsten layer 9 that overlies a tungsten nitride layer 11. Other conductive (stack) materials, such as tungsten silicide or cobalt silicide, are also used.

          One of the problems with this approach is that the conductive stack 13 may promote cross-diffusion. Cross-diffusion occurs when impurities from one type of

5 polycrystalline silicon diffuse up to the conductive stack 13 and diffuse down to the other type of polycrystalline silicon. This movement of impurities undesirably transforms the designed semiconductor characteristic of the polycrystalline silicon. Another problem is that certain conductive materials may decompose during processing, which forms an undesired nonconductive layer that may degrade performance of a semiconductor device. For example, the tungsten layer 9 must be used with the tungsten nitride layer 11, but the tungsten nitride layer 11 may react with either of the polycrystalline silicon strips 10A, B to form silicon nitride, which is a nonconductive compound. This nonconductive compound may increase the vertical resistance of the gate stack 15, and thereby, may degrade the speed at which a semiconductor device that includes the gate stack 15 can operate. To avoid this increase in the vertical resistance, some semiconductor manufacturers have supplanted the use of the tungsten layer 9 and the tungsten nitride layer 11 with a layer of cobalt silicide, tungsten silicide, or titanium silicide, but in so doing, one problem is replaced with another problem. The cobalt silicide may increase the horizontal resistance of the gate stack 15 compared to the tungsten layer 9, and once again, the operational speed of the semiconductor device using the gate stack 15 may be degraded.

20 If the operational speed of the semiconductor devices is degraded, the operational speed of circuits that are built from these semiconductor devices may be degraded as well. However, certain circuits often need to quickly process signals, such as timing, address, and data. Without the means to solve the problems discussed above, the operational speed of these semiconductor devices may be less than desired, which may lead to their eventual lack of acceptance in the marketplace. Thus, there is a need for structures and methods to enhance semiconductor structures to inhibit cross-diffusion and decrease vertical and horizontal resistance so that semiconductor devices, which are built upon these semiconductor structures, may operate at high speed.

## 30 SUMMARY OF THE INVENTION

One illustrative aspect includes a method for strapping a gate structure of a transistor in a periphery area of a semiconductor structure. The method includes forming from a nonconductive stack a trench that superjacently abuts along a substantially length of a dual-doped

5 polycrystalline silicon line having a p-type strip abutting an n-type strip. The nonconductive  
stack includes a stopping layer that stops an etching process once etched away to define the  
bottom of the trench. The method further includes filling the trench with a conductive substance  
to strap the dual-doped polycrystalline silicon line. The trench has a large cross-sectional area to  
decrease a horizontal resistance of the transistor so as to increase the performance of the  
10 transistor.

#### BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1A-1B are cross-sectional views of a conventional semiconductor structure.

15 Figure 2 is a cross-sectional view of a semiconductor structure according to one embodiment of the present invention.

Figures 3A-3P are cross-sectional views of a semiconductor structure during processing according to various embodiments of the present invention.

20 Figure 4 is a plan view of a semiconductor wafer according to one embodiment of the present invention.

Figure 5 is a block diagram of a circuit module according to one embodiment of the present invention.

Figure 6 is a block diagram of a memory module according to one embodiment of the present invention.

25 Figure 7 is a block diagram of an electronic system according to one embodiment of the present invention.

Figure 8 is a block diagram of a memory system according to one embodiment of the present invention.

30 Figure 9 is a block diagram of a computer system according to one embodiment of the present invention.

## 5 DETAILED DESCRIPTION OF THE INVENTION

In the following detailed description of various embodiments of the invention, reference is made to the accompanying drawings, which form a part hereof, and in which are shown, by way of illustration, specific embodiments in which the invention may be practiced. In the drawings, like numerals describe substantially similar components throughout the several  
10 views. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and structural, logical, electrical, and other changes may be made without departing from the spirit or scope of the present invention. The following detailed description is, therefore, not to be taken in a limiting sense.

A semiconductor structure, such as a memory device, may have both an array of  
15 memory cells and peripheral circuits. The array of memory cells store information, and may be referred to as an array or a storage aspect. The array may require high density so that a large amount of information may be stored within a limited amount of space. The peripheral circuits often need to quickly process signals, such as timing, address, and data, so as to access the array to read or to write information. Such peripheral circuits may be referred to as a periphery or a  
20 logic aspect of a memory device. The periphery may require high speed to keep up with the demand of a fast central processing unit. Thus, both high speed and high density are desired for memory devices. Figure 2 is a cross-sectional view of a semiconductor structure 100 illustrating both the array and the periphery according to one embodiment of the present invention.

The semiconductor structure 100 may represent a portion of a memory device,  
25 such as a static RAM (SRAM) module. The semiconductor structure 100 includes a high-density area, which may be part of an array 102, and a high-speed area, which comprises peripheral circuitry, and may be referred to collectively as a periphery 103. The array 102 includes a number of devices, such as memory cells, that coexist in close proximity with each other. For brevity purposes, only one device, which is represented by a gate structure 106, is shown in the  
30 array 102. The periphery 103 also includes a number of devices that operate at high speed, such as timing circuits and decoders. For brevity purposes, two devices, which are represented by a gate structure 108 and a gate structure 110, are shown in the periphery 103.

Gate structures 106, 108, and 110 in the array 102 and the periphery 103 are built upon a substrate 104. The substrate 104 includes active areas, which are highly doped regions that form sources and drains, and inactive areas, which are field regions. For clarity purposes, the active and inactive areas are not shown so as to focus on the gate structures 106, 108, and 110. The gate structures 106, 108, and 110 each include a gate oxide layer 112, a polycrystalline silicon layer 114, a conductive layer 116, a gate cap layer 118, and spacers 120. A nonconductive layer 122, such as borophosphorus silicate glass (BPSG), isolates the gate structures of the devices 106, 108, and 110.

A metallization layer, which is identified collectively by numerical nomenclatures 124<sub>1</sub>, 124<sub>2</sub>, 124<sub>3</sub>, and 124<sub>4</sub>, fills a number of openings, such as openings 126<sub>1</sub>, 126<sub>2</sub>, and 126<sub>3</sub>, that open to certain portions of gate structures 106, 108, and 110, including a via 125. The metallization layer 124<sub>1</sub> acts as a local interconnect to electrically couple an active portion of the substrate 104, such as a drain or a source, to the polycrystalline silicon layer 114. The metallization layer 124<sub>2</sub> acts as a strap to the polycrystalline silicon layer 114. The metallization layer 124<sub>3</sub> acts as a routing for a conductive path that overlies the gate structure 110. The metallization layer 124<sub>4</sub> allows access to another active portion of the substrate 104, such as a drain or a source, by way of the via 125.

The openings 126<sub>1</sub>, 126<sub>2</sub>, and 126<sub>3</sub> are formed using a suitable high-density fabrication technique. One suitable technique includes a self-aligned contact (SAC) etching technique. In the array 102, this technique builds high-density semiconductor devices, such as memory cells. In the periphery 103, this technique provides a generous margin to form the metallization layer 124<sub>2</sub> which straps to certain areas in the polycrystalline silicon layer 114.

Each of the metallization layers 124<sub>1</sub>, 124<sub>2</sub>, 124<sub>3</sub>, and 124<sub>4</sub> includes several layers, such as a silicide layer 128, a conductor layer 130, and/or a barrier layer (not shown). The silicide layer 128 lowers the vertical resistance of a metal/semiconductor junction, which is a contact point between one of the metallization layers and a gate, source, or drain of a transistor. The conductor layer 130 may be formed from a substance that lowers the horizontal resistance; this substance includes a refractory metal, such as tungsten. Depending on the substance chosen

5 for the conductor layer 130, a barrier layer may be formed so as to inhibit undesired diffusion among the several layers of the metallization layers 124<sub>1</sub>, 124<sub>2</sub>, 124<sub>3</sub>, and 124<sub>4</sub>.

Figures 3A-3P are cross-sectional views of the semiconductor structure 100 during processing according to one embodiment of the present invention. The discussion in Figures 3A-3P illustrates a few of the steps associated with a fabrication process. The entire  
10 fabrication process is not discussed so as to focus on the embodiments of the present invention. Other methods of fabrication are also feasible and perhaps equally viable. For clarity purposes, many of the reference numbers, once discussed, may be eliminated from subsequent drawings so as to provide greater emphasis on the portion of interest of the semiconductor structure 100.

Figure 3A is a cross-sectional view of the semiconductor structure 100 during  
15 processing according to one embodiment of the present invention. The gate oxide layer 112 is grown over the substrate 104 and covers the array 102 as well as the periphery 103. Any suitable technique can be used to grow the gate oxide layer 112. One suitable technique includes exposing the substrate 104 to dry oxygen at 900 degrees Celsius for one hour, which is followed by an annealing process in argon for 30 minutes.

20 Other processing steps may be applied prior to or after the formation of the gate oxide layer 112, but these steps do not limit the embodiments of the present invention, and thus, are not shown so as to focus on the embodiments of the present invention. Briefly, the substrate 104 can be formed from any suitable substances and compounds, such as lightly doped n-type or p-type material or a lightly doped epitaxial layer on a heavily doped substrate. Field oxide may  
25 be deposited, patterned, and etched on the substrate 104 so as to define non-active areas of the substrate 104.

Figure 3B is a cross-sectional view of the semiconductor structure 100 during the next sequence of processing according to one embodiment of the present invention. A polycrystalline silicon layer 114 is deposited over the semiconductor structure 100 after the gate  
30 oxide layer 112 is formed. This polycrystalline silicon layer 114 is photolithographed and is etched at selected areas on the substrate 104 to form gate structures in the array 102 and the periphery 103. The etching process etches away not only portions of the polycrystalline silicon

5 layer 114 but also portions of the gate oxide layer 112 to define the beginning of gate structures 106, 108, and 110.

Other processing steps may be applied prior to or after the formation of the polycrystalline silicon layer 114, but these steps do not limit the embodiments of the present invention, and thus, are not shown so as to focus on the embodiments of the present invention.

10 For example, impurities of the appropriate kind are implanted into the source and drain areas so as to form highly doped regions that provide a reservoir of majority carriers for the conduction of holes or electrons. Reoxidation of the source and drain areas to pattern gate areas may follow the implantation step.

Any suitable technique may be used to deposit the polycrystalline silicon layer

15 114. One suitable technique includes chemical-vapor deposition. Any suitable technique may be used to etch the polycrystalline silicon layer 114 and the gate oxide layer 112. One suitable technique includes a plasma etching technique. Other deposition techniques and etching techniques may be used without limiting the embodiments of the present invention.

Figure 3C is a cross-sectional view of the semiconductor structure 100 during the

20 next sequence of processing according to one embodiment of the present invention. A conductive layer 116 is deposited, photolithographed, and etched over the semiconductor structure 100 to provide a number of metal/semiconductor junctions to gate structures 106, 108, and 110. These junctions allow electrical access to the gate structures 106, 108, and 110. In other words, these junctions allow word lines to be electrically coupled to the gate structures 106,

25 108, and 110.

If the conductive layer 116 has a high likelihood of diffusing to the polycrystalline silicon layer 114, a barrier layer 115 can be used to inhibit the diffusion. In cases where the barrier layer 115 is needed, the barrier layer 115 is deposited first prior to the deposition of the conductive layer 116. Any suitable deposition technique to deposit the conductive layer 116 or

30 the barrier layer 115 may be used. One suitable technique includes sputtering. Any suitable etching technique may be used to etch the conductive layer 116 or the barrier layer 115, such as plasma etching. Suitable conductive materials include tungsten or various species of tungsten silicide. Suitable barrier materials include various species of tungsten nitride. Many other



5     suitable conductive materials and barrier materials may be used without limiting the  
embodiments of the present invention.

Figure 3D is a cross-sectional view of the semiconductor structure 100 during the  
next sequence of processing according to one embodiment of the present invention. A dielectric  
layer 118 is deposited, photolithographed, and etched to cap the gate structures 106, 108, and  
10     110. A suitable dielectric material includes silicon dioxide, but any other suitable dielectric  
materials may be used. A suitable deposition technique includes chemical-vapor deposition and  
a suitable etching technique includes plasma etching. Other suitable deposition and etching  
techniques may be used without limiting the embodiments of the present invention.

Figure 3E is a cross-sectional view of the semiconductor structure 100 during the  
15     next sequence of processing according to one embodiment of the present invention. The  
semiconductor structure 100 undergoes a photolithography process to simultaneously expose  
desired areas in the array 102 and the periphery 103. More particularly, the photolithography  
process exposes a portion of the gate structure 106, which is in the array 102, and a portion of the  
gate structure 108, which is in the periphery 103, so that openings 127<sub>1</sub> and 127<sub>2</sub> may be formed  
20     at a desired depth into these gate structures. In one embodiment, the photolithography process  
exposes at least the opening 127<sub>2</sub>.

The opening 127<sub>1</sub> into the portion of the gate structure 106 helps to exhumate  
contact with the polycrystalline silicon layer 114. The opening 127<sub>2</sub> into the portion of the gate  
structure 108 allows the polycrystalline silicon layer 114 to be strapped by a metallization layer.  
25     This photolithography process contributes to economizing the formation of openings 127<sub>1</sub> and  
127<sub>2</sub> in both the array 102 and the periphery 103, which will be discussed hereinbelow in other  
Figures.

The photolithography process deposits a resist layer 119. This resist layer 119 is  
exposed to ultraviolet light through a mask, and the exposed regions are dissolved by a  
30     developing solution. The remaining resist layer 119 serves as a mask for etching to form  
openings 127<sub>1</sub> and 127<sub>2</sub> into gate structures 106 and 108.

Figure 3F is a cross-sectional view of the semiconductor structure 100 during the  
next sequence of processing according to one embodiment of the present invention. The

5 semiconductor structure 100 is etched to remove exposed portions of the gate structures 106 and 108 so that openings 127<sub>1</sub> and 127<sub>2</sub> are formed. Thus, the etching process may remove portions of the dielectric layer 118, conductive layer 116, and/or barrier layer 115. A portion of the resist layer 119 that was not removed by the developing solution remains to serve as a mask to guide the etching process. One suitable etching process includes a dry-etch technique, such as plasma,  
10 ion milling, or reactive ion etching.

Figure 3G is a cross-sectional view of the semiconductor structure 100 during the next sequence of processing according to one embodiment of the present invention. The resist 119 that serves as a mask to guide the etching process in Figure 3F is stripped using any suitable stripping technique. One suitable technique includes a wet chemical stripping technique using  
15 sulfuric acid and oxidant solutions. Another suitable technique includes a dry stripping technique, such as a plasma process.

Figure 3H is a cross-sectional view of the semiconductor structure 100 during the next sequence of processing according to one embodiment of the present invention. A thick oxide layer 120 is deposited over the semiconductor structure 100 and anisotropically etched  
20 away to leave only the sidewall spacers as shown in the Figure 2H. One suitable deposition technique to deposit the thick oxide layer includes a low-temperature chemical-vapor deposition technique.

Figure 3I is a cross-sectional view of the semiconductor structure 100 during the next sequence of processing according to one embodiment of the present invention. An etch  
25 stopping layer 121 is deposited over the semiconductor structure 100 as shown in Figure 3I. The next time the semiconductor structure 100 undergoes an etching process, the etching process will etch away the stopping layer 121, but in so doing, the etching process will cease from removing any other layers subjacent the stopping layer 121.

The stopping layer 121 may be deposited using a suitable material, such as a  
30 dielectric liner. The dielectric liner can be chosen from silicon dioxide, which is derived from tetraethylorthosilicate (TEOS). Any suitable deposition technique may be used, such as hot-wall low-pressure chemical-vapor deposition. Another suitable material is a dielectric-antireflective-

5 coating (DARC) compound, such as inorganic silicon oxynitride (SiON), which can be deposited using a suitable technique, such as plasma-enhanced chemical-vapor deposition (PECVD).

Figure 3J is a cross-sectional view of the semiconductor structure 100 during the next sequence of processing according to one embodiment of the present invention. A layer of borophosphosilicate glass (BPSG) 122 is deposited over the semiconductor structure 100 to  
10 provide mechanical protection and electrical isolation for gate structures 106, 108, and 110. One suitable deposition technique includes chemical-vapor deposition.

Figure 3K is a cross-sectional view of the semiconductor structure 100 during the next sequence of processing according to one embodiment of the present invention. The semiconductor structure 100 undergoes a photolithography process in which a resist layer 123 is  
15 deposited and is exposed to ultraviolet light through a mask. The exposed regions are dissolved by a developing solution. The remaining resist layer 123 that is still attached to the semiconductor structure 100 after developing serves as a mask. The mask is used to expose certain areas of the semiconductor structure 100 for etching to form openings 126<sub>1</sub>, 126<sub>2</sub>, 126<sub>3</sub>, and 126<sub>4</sub> as will be explained with respect to Figure 3L.

20 Figure 3L is a cross-sectional view of the semiconductor structure 100 during the next sequence of processing according to one embodiment of the present invention in which the semiconductor structure 100 undergoes an etching process to form openings 126<sub>1</sub>, 126<sub>2</sub>, 126<sub>3</sub>, and 126<sub>4</sub>. The portions of the resist layer 123 that were not removed by the developing solution remain to serve as a mask to guide the etching process to form openings 126<sub>1</sub>, 126<sub>2</sub>, 126<sub>3</sub>, and  
25 126<sub>4</sub>. Thus, the etching process may remove portions of the BPSG layer 122 and the stopping layer 121 to stop at the dielectric layer 118, polycrystalline silicon layer 114, or the substrate 104. One suitable etching process includes a dry-etch technique, such as plasma, ion milling, or reactive ion etching.

After the formation of the openings 126<sub>1</sub>, 126<sub>2</sub>, 126<sub>3</sub>, and 126<sub>4</sub>, the resist layer 123  
30 that serves as a mask to guide the etching process is stripped using any suitable stripping technique. One suitable technique includes a wet chemical stripping technique using sulfuric acid and oxidant solutions. Another suitable technique includes a dry stripping technique, such as a plasma process. The result of the etching and stripping processes is shown in Figure 3L.

5           The opening 126<sub>1</sub> creates a local interconnect between a portion of the gate structure 106 and a highly doped area (not shown) in the polycrystalline silicon layer 114. The opening 126<sub>2</sub> allows the polycrystalline silicon layer 114 to be strapped by a metallization layer if the polycrystalline silicon layer is a dual-doped polycrystalline silicon layer used for complementary semiconductor structures, such as complementary-metal-oxide semiconductor  
10 (CMOS) devices. The opening 126<sub>3</sub> allows local routing over the gate structure 110. The opening 126<sub>4</sub> allows electrical access to a highly doped area of the substrate 104. This photolithography process economizes the formation of openings 126<sub>1</sub>, 126<sub>2</sub>, and 126<sub>3</sub> in both the array 102 and the periphery 103 so that the embodiments of the present invention may provide a metallization layer, which will be discussed hereinbelow in other Figures, to enhance high-speed  
15 operation, support high-density devices, and inhibit undesired cross-diffusion.

          In the idiom of semiconductor processing, the sequence of processing as discussed in Figures 3K-3L is called a self-aligned contact (SAC) etching technique. This SAC etching technique takes advantage of the fact that memory cells have similar features, which allows them to be produced with a high density. Although this SAC etching technique has been adopted by  
20 the semiconductor manufacturers to increase density in the array, they have refrained from using it to fabricate circuitry in the periphery, which comprises high-speed devices, because they believe that the process adds too much complexity. The embodiments of the present invention recognize that not only this technique can be used to build the high-density array 102 but it can also be used to extend into the high-speed periphery 103 to create various openings for  
25 metallization. One way that the SAC etching technique helps to increase performance is to allow a thicker metallization layer (or larger cross-sectional area) to be deposited into the opening 126<sub>2</sub> to strap the polycrystalline silicon layer 114. Because horizontal resistivity is inversely proportional to the cross-sectional area, this increase in the cross-sectional area helps to increase performance.

30           Figure 3M is a cross-sectional view of the semiconductor structure 100 during the next sequence of processing according to one embodiment of the present invention. A conductive layer 129 is deposited over the semiconductor structure 100, which can be reacted with to form a silicide compound in exposed regions of polycrystalline silicon or highly doped

5 areas of the substrate 104. The silicide compound helps to reduce vertical resistance that may exist in vertically oriented gate structures, such as gate structures 106, 108, and 110. The conductive layer 129 includes a number of substances, such as platinum, molybdenum, cobalt, and titanium.

The discussion in Figure 3M is better understood by explaining the physics by  
 10 which the silicide compound helps to reduce vertical resistance. To access a semiconductor device, a metal/semiconductor junction is formed so that a contact can be made. Unlike a semiconductor/semiconductor junction, such as exists in a diode, a metal/semiconductor junction may present a potential barrier that affects the transport of charges, and hence, impairs the ability of the semiconductor device to operate at high speed. To increase the speed, this potential barrier  
 15 should be lowered. One technique to lower this potential barrier is to form a silicide layer that interfaces between the metal and the semiconductor. This silicide layer lowers the work function so as to ease the ability of the electrons to move across the metal/semiconductor junction.

One benefit of the technique as described in Figure 3M is that the conductive layer 129 is simultaneously deposited throughout desired sections in both the array 102 and the  
 20 periphery 103, where a silicide compound 128 as best shown in Figure 3N can be formed. The silicide compound 128 not only helps to facilitate high-speed operation in the periphery area 103, such as in the conduction of carriers in the via 125, but is also a part of a local interconnect material used in the array area 102, such as in the opening 126<sub>1</sub>.

Figure 3N is a cross-sectional view of the semiconductor structure 100 during the  
 25 next sequence of processing according to one embodiment of the present invention in which a barrier layer 131 is optionally deposited. A barrier layer 131 inhibits the undesired diffusion of metal atoms into a silicon crystal structure. One suitable technique to deposit the barrier layer includes a sputtering process. The material of the barrier layer 131 may include various species of nitrides, such as titanium nitride and tantalum nitride, or titanium-tungsten.

30 The conductive layer 129 is then reacted with through an annealing process to form a silicide compound 128 throughout the array 102 and the periphery 103. The conductive layer 129 may undergo the annealing process at this step, or at any time before the completion of the processing of the semiconductor structure 100. The remaining unreacted conductive layer

5 129 is then removed. The result is as shown in Figure 3N. In other cases, the unreacted conductive layer is left on the wafer surface, which is followed by deposition of a conductive barrier layer before depositing the conductive layer 133.

Figure 3O is a cross-sectional view of the semiconductor structure 100 during the next sequence of processing according to one embodiment of the present invention. A  
 10 conductive layer 133 is deposited over both the array 102 and the periphery 103. The conductive layer 133 is chosen from a substance that can be used simultaneously for a variety of purposes: as a local interconnect in the openings 126<sub>1</sub> for the gate structure 106 in the array 102; as a strap in the openings 126<sub>2</sub> for the gate structure 108 in the periphery 103; as a routing conductor in the opening 126<sub>3</sub> which lies over the gate structure 110 in the periphery 103; and as a plug material  
 15 for the via 125. This substance also acts to reduce the horizontal resistance (sheet resistance) so as to enhance high-speed operation in the periphery 103.

The conductive layer 133 is chosen from a substance that includes a representative metal, such as aluminum; a refractory metal, such as tungsten; or a coinage metal, such as copper. Any suitable deposition technique can be used to deposit the conductive layer 133, such  
 20 as sputtering.

Figure 3P is a cross-sectional view of the semiconductor structure 100 during the next sequence of processing according to one embodiment of the present invention in which the conductive layer 133 undergoes a chemical-mechanical planarization process. The result is as shown in Figure 3P.

25 Surface p-channel transistors, such as represented by gate structure 108, are compatible with the need to scale down to the smaller dimensions. Semiconductor manufacturers use both n<sup>+</sup> and p<sup>+</sup> polycrystalline silicon gates on the same chip so as to form these surface n-channel and p-channel transistors. The technique of using both n<sup>+</sup> and p<sup>+</sup> polycrystalline silicon is called a dual-doped approach, and to prevent an undesired diode from  
 30 forming at the interface of the n<sup>+</sup> and p<sup>+</sup> polycrystalline, the n<sup>+</sup> polycrystalline is strapped to the p<sup>+</sup> polycrystalline. However, this technique often suffers from cross-diffusion when the semiconductor structure undergoes high temperature processing steps. The embodiments of the present invention overcome this by forming the metallization layer, which includes conductive

5 layer 133, barrier layer 131, and silicide layer 128, near the completion of the semiconductor structure 100 so as to avoid high temperature processing steps.

Figure 4 is a plan view of a semiconductor wafer according to one embodiment of the present invention. In one embodiment, a semiconductor die 610 is produced from a wafer 600. A die is an individual pattern, typically rectangular, on a substrate that contains circuitry, or  
10 integrated circuit devices, to perform a specific function. At least one of the integrated circuit devices includes a semiconductor structure 100 as discussed in the various embodiments hereinbefore in accordance with the invention. A semiconductor wafer will typically contain a repeated pattern of such dies containing the same functionality. Die 610 may contain circuitry for the inventive memory device, as discussed above. Die 610 may further contain additional  
15 circuitry to extend to such complex devices as a monolithic processor with multiple functionalities. Die 610 is typically packaged in a protective casing (not shown) with leads extending therefrom (not shown) providing access to the circuitry of the die for unilateral or bilateral communication and control.

Figure 5 is a block diagram of a circuit module according to one embodiment of  
20 the present invention. Two or more dies 710 may be combined, with or without protective casing, into a circuit module 700 to enhance or extend the functionality of an individual die 710. Circuit module 700 may be a combination of dies 710 representing a variety of functions, or a combination of dies 710 containing the same functionality. One or more dies 710 of circuit module 700 contain at least a semiconductor structure 100 in accordance with the embodiments  
25 of the present invention.

Some examples of a circuit module include memory modules, device drivers, power modules, communication modems, processor modules, and application-specific modules, and may include multiplayer, multichip modules. Circuit module 700 may be a subcomponent of a variety of electronic systems, such as a clock, a television, a cell phone, a personal computer,  
30 an automobile, an industrial control system, an aircraft, and others. Circuit module 700 will have a variety of leads 712 extending therefrom and coupled to the dies 710 providing unilateral or bilateral communication and control.

5           Figure 6 is a block diagram of a memory module according to one embodiment of the present invention. Memory module 800 contains multiple memory devices 810 contained on support 815, the number depending upon the desired bus width and the desire for parity. Memory module 800 accepts a command signal from an external controller (not shown) on a command link 820 and provides for data input and data output on data links 830. The command  
10 link 820 and data links 830 are connected to leads 840 extending from the support 815. Leads 840 are shown for conceptual purposes and are not limited to the positions as shown. At least one of the memory devices 810 includes a semiconductor structure 100 as discussed in various embodiments in accordance with the invention.

          Figure 7 is a block diagram of an electronic system according to one embodiment  
15 of the present invention. Electronic system 900 contains one or more circuit modules 902. Electronic system 900 generally contains a user interface 904. User interface 904 provides a user of the electronic system 900 with some form of control or observation of the results of the electronic system 900. Some examples of user interface 904 include the keyboard, a pointing device, monitor, or printer of a personal computer; the tuning dial, display, or speakers of a radio;  
20 the ignition switch, gauges, or gas pedal of an automobile; and the card reader, keypad, display, or currency dispenser of an automated teller machine. User interface 904 may further describe access ports provided to electronic system 900. Access ports are used to connect an electronic system to the more tangible user interface components previously exemplified. One or more of the circuit modules 902 may be a processor providing some form of manipulation, control, or  
25 direction of inputs from or outputs to user interface 904, or of other information either preprogrammed into, or otherwise provided to, electronic system 900. As will be apparent from the lists of examples previously given, electronic system 900 will often contain certain mechanical components (not shown) in addition to circuit modules 902 and user interface 904. It will be appreciated that the one or more circuit modules 902 in electronic system 900 can be  
30 replaced by a single integrated circuit. Furthermore, electronic system 900 may be a subcomponent of a larger electronic system. At least one of the circuit modules 902 includes a semiconductor structure 100 as discussed in various embodiments in accordance with the invention.



5           Figure 8 is a block diagram of a memory system according to one embodiment of the present invention. Memory system 1000 contains one or more memory modules 1002 and a memory controller 1012. Each memory module 1002 includes at least one memory device 1010. Memory controller 1012 provides and controls a bi-directional interface between memory system 1000 and an external system bus 1020. Memory system 1000 accepts a command signal from the  
10 external bus 1020 and relays it to the one or more memory modules 1002 on a command link 1030. Memory system 1000 provides for data input and data output between the one or more memory modules 1002 and external system bus 1020 on data links 1040. At least one of the memory devices 1010 includes a semiconductor structure 100 as discussed in various embodiments in accordance with the invention.

15           Figure 8 is a block diagram of a computer system according to one embodiment of the present invention. Computer system 1000 contains a processor 1110 and a memory system 1102 housed in a computer unit 1105. Computer system 1100 is but one example of an electronic system containing another electronic system, e.g., memory system 1102, as a subcomponent. The memory system 1102 may include a semiconductor structure 100 as  
20 discussed in various embodiments of the present invention. Computer system 1100 optionally contains user interface components. These user interface components include a keyboard 1120, a pointing device 1130, a monitor 1140, a printer 1150, and a bulk storage device 1160. It will be appreciated that other components are often associated with computer system 1100 such as modems, device driver cards, additional storage devices, etc. It will further be appreciated that  
25 the processor 1110 and memory system 1102 of computer system 1100 can be incorporated on a single integrated circuit. Such single-package processing units reduce the communication time between the processor and the memory circuit.

          Devices, structures, and methods have been discussed to address a desire to have a semiconductor structure with both a high-density aspect and a high-speed aspect. The  
30 embodiments of the present invention use a SAC etching technique not only to form high-density devices but also to form openings so that a metallization layer may be deposited to lower horizontal resistance and vertical resistance to enhance high-speed operation. The embodiments

5 of the present invention economize the manufacturing of semiconductor devices by simplifying processing steps so as to produce less expensive products for consumers.

Although the specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiments shown. This  
10 application is intended to cover any adaptations or variations of the present invention. It is to be understood that the above description is intended to be illustrative, and not restrictive. Combinations of the above embodiments and other embodiments will be apparent to those of skill in the art upon reviewing the above description. The scope of the invention includes any other applications in which the above structures and fabrication methods are used. Accordingly,  
15 the scope of the invention should only be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.